Physical ASIC Design Implementation Engineer

About the company

Qplox is a fast-growing company offering test and automation engineering. Headquartered in Leuven, with offices in Barcelona and Eindhoven.
Our clients are major multinational enterprises and local companies from automotive, semiconductors, RF, consumer electronics…. Our Test automation group offers a one stop shop for design of automated test benches, system integration production, lab automation and data acquisition systems, with a growing focus in IoT sensor networks.
Our consultancy department offers services in RF, semiconductors and electronics design and test, as well as on the crossing roads of Nanotechnology, Bio-Science Engineering and Biotechnology.

Job Description

We are currently looking for a Physical Implementation engineer for full backend (P&R) projects from netlist-in to GDSII-out flow, for top level chips as well as block level blocks in technologies ranging from N5 to 180nm. This with the full understanding of the complete Cadence Innovus Place&Route flow.

In this assignment the selected candidate will be involved in:

- Setup of full netlist In to GDSII-out P&R flow (libs, derating, low power,..).
- Place&Route : from floorplanning untill postroute.
- Solve setup/hold/SI/power/... violations.
- Signoff Timing and Physical/logical verification (LEC, DRC, LVS,...).
- Discuss constraints/specs with, feedback results to and cooperate with customer.

Location: Leuven

Candidate Description

- You have 10 years of experience in physical implementation in advanced nodes (12 – 7nm) and hierarchical designs.
- You have experience in debugging capabilities.
- You have experience with tcl scripting.
- You can organize your work flexible, and make sure the progress in the project is running smooth.
- To be able to communicate in English is a must, you will also interact with external customers.
- You function well in an international team.

We offer

An attractive salary package with extra benefits. A high tech, multicultural and young ambient. A fast track in a growing company. Formation in multidisciplinary environment plenty of learning opportunities.

Contact

Send your CV and application letter to jobs@qplox.com with the subject "**Physical ASIC Design Implementation Engineer".**